

FIG. 1

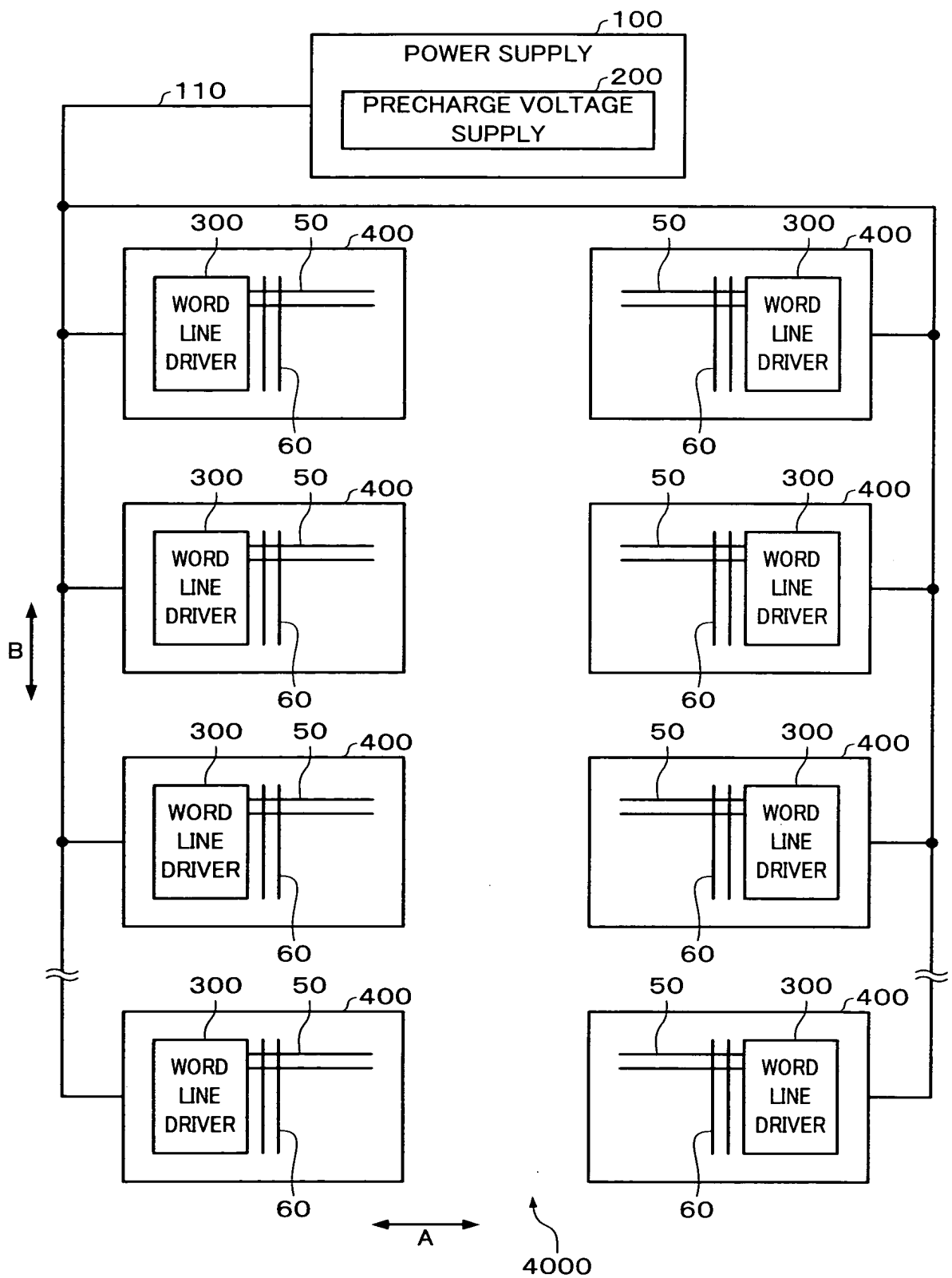


FIG. 2

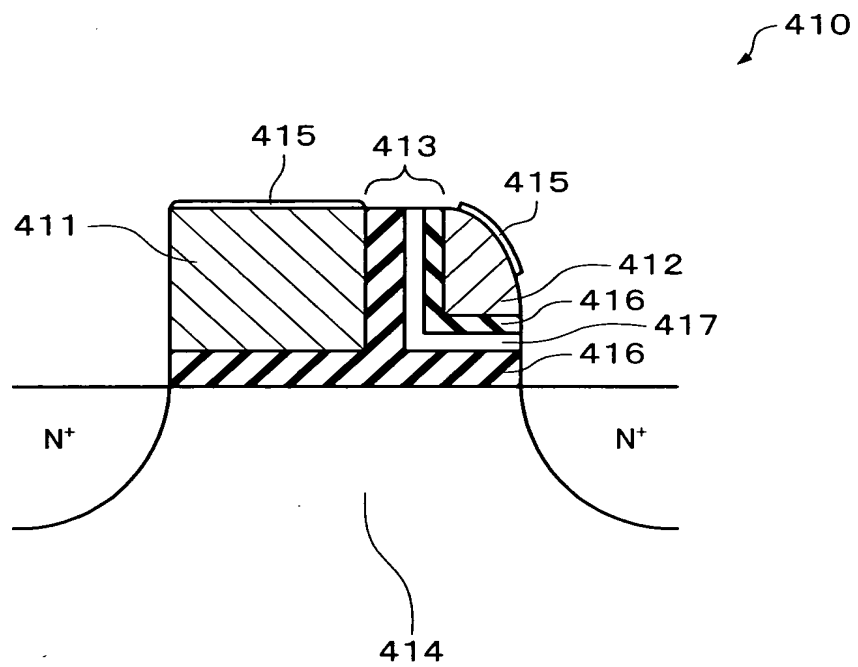


FIG. 3

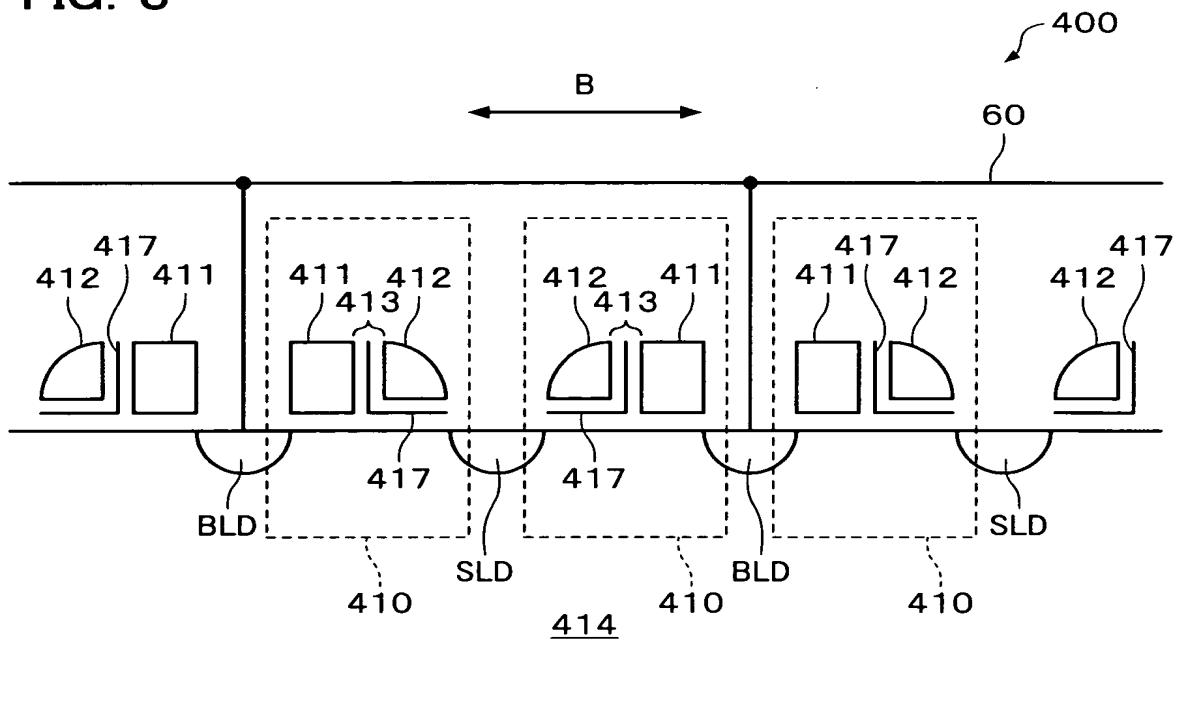


FIG. 4

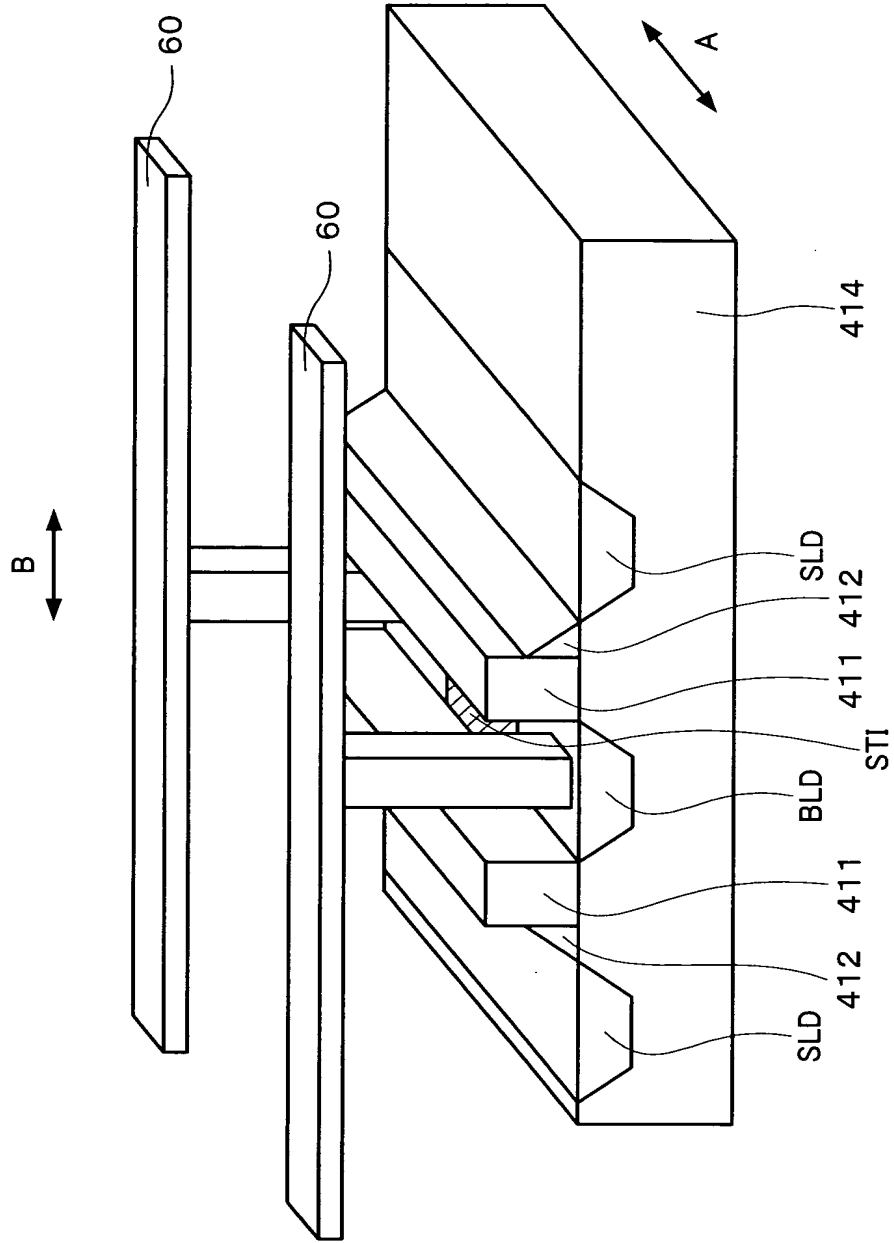


FIG. 5

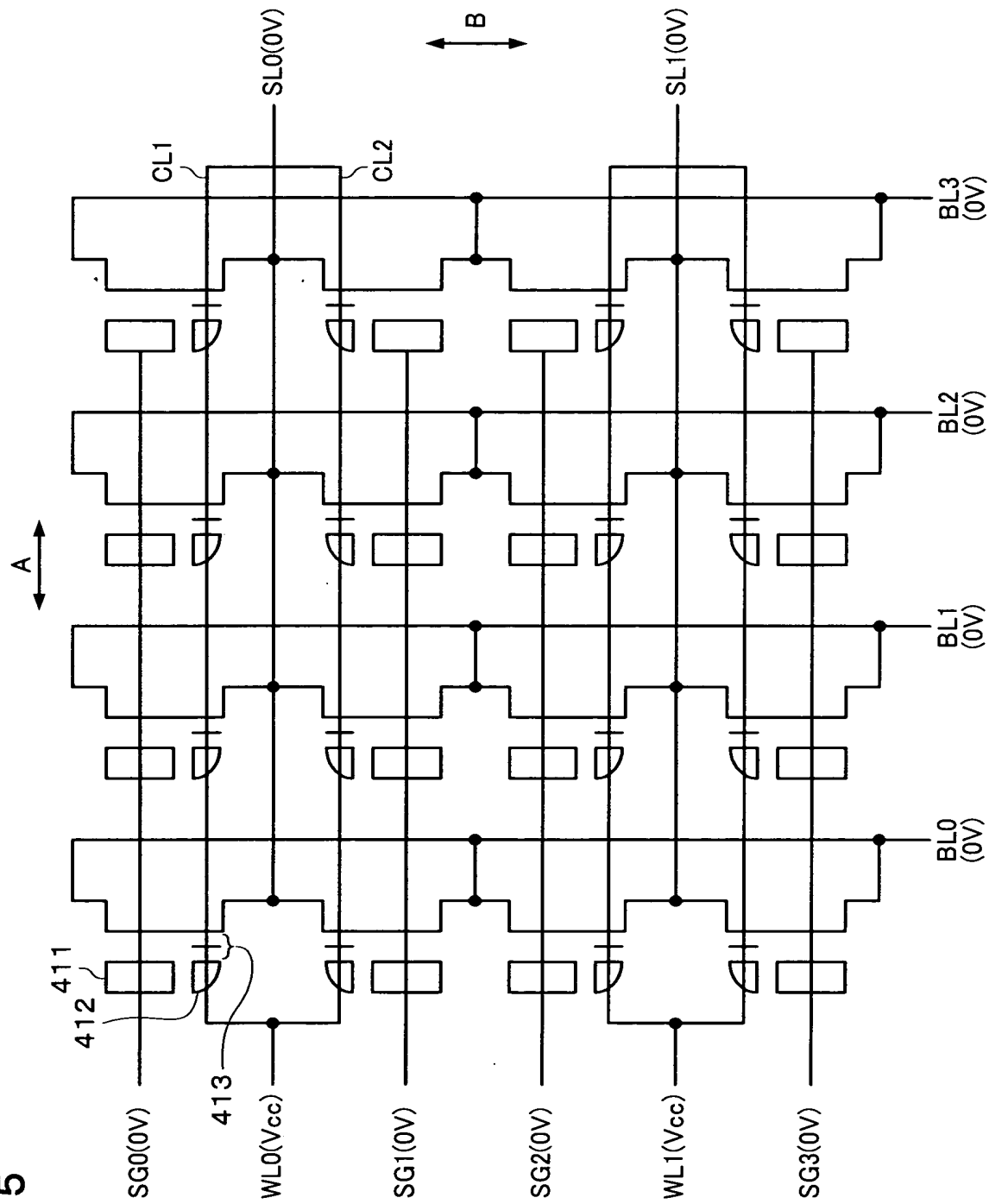


FIG. 6

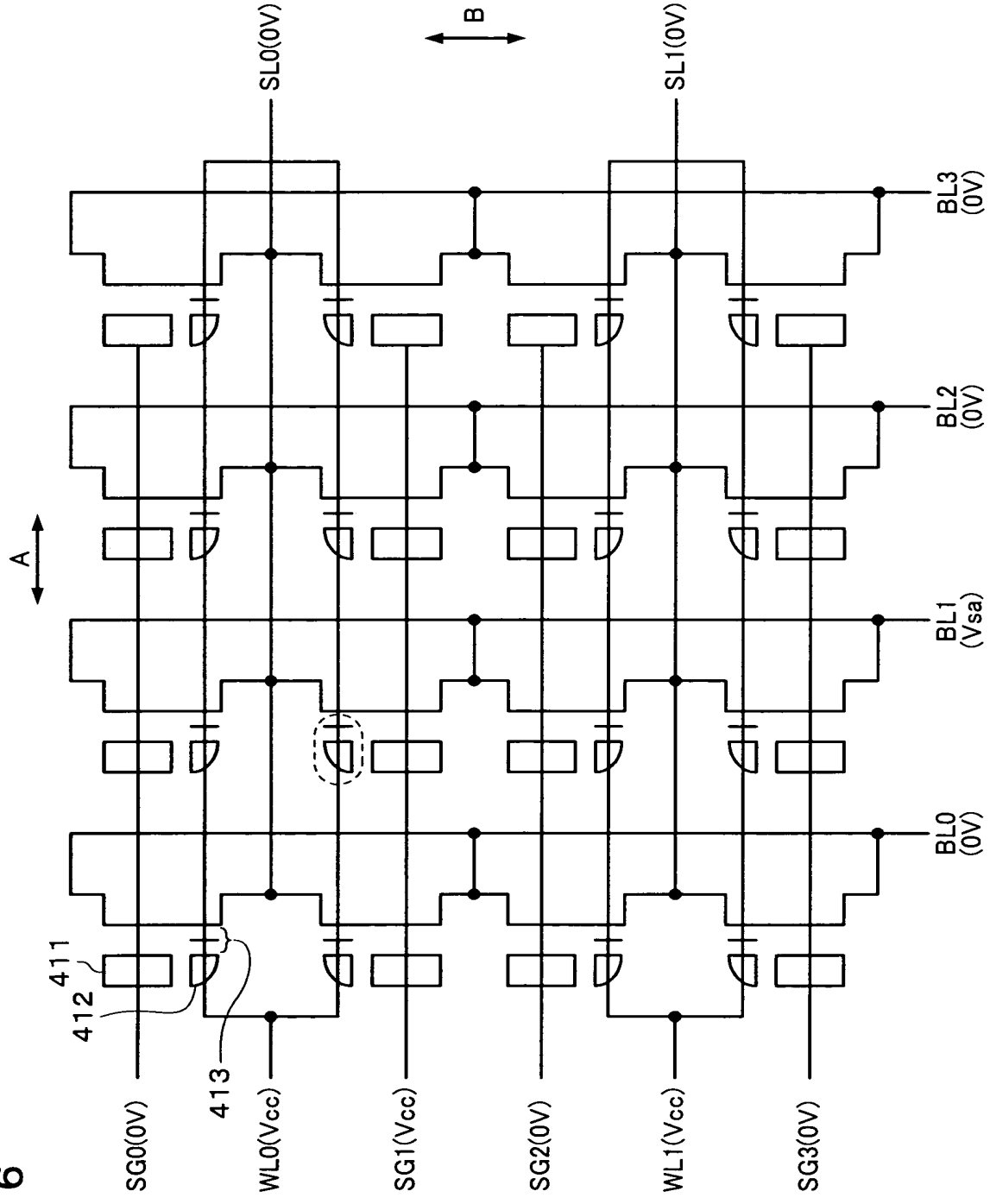


FIG. 7

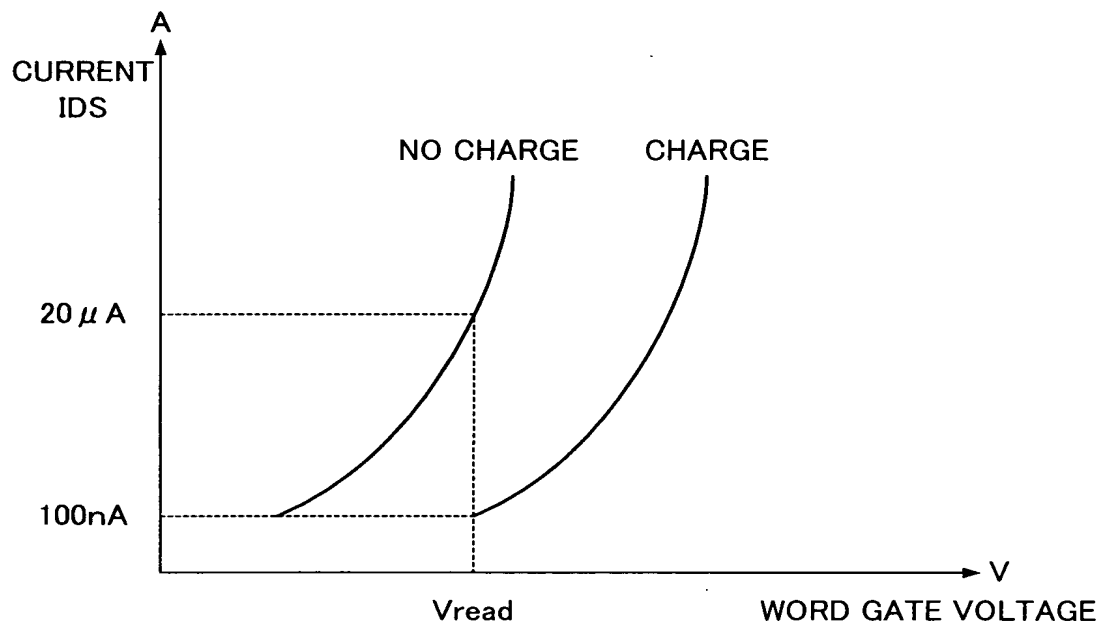


FIG. 8

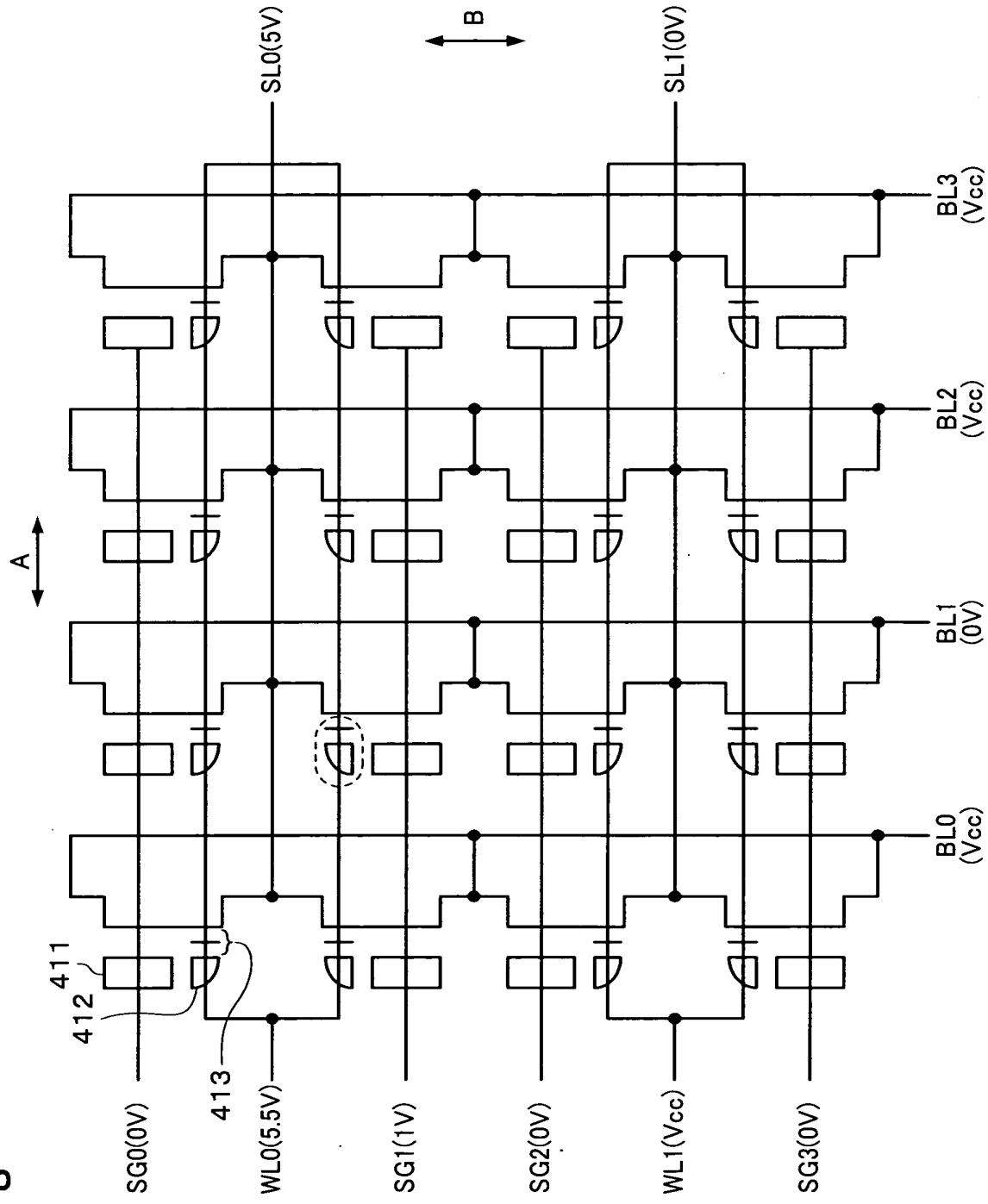


FIG. 9

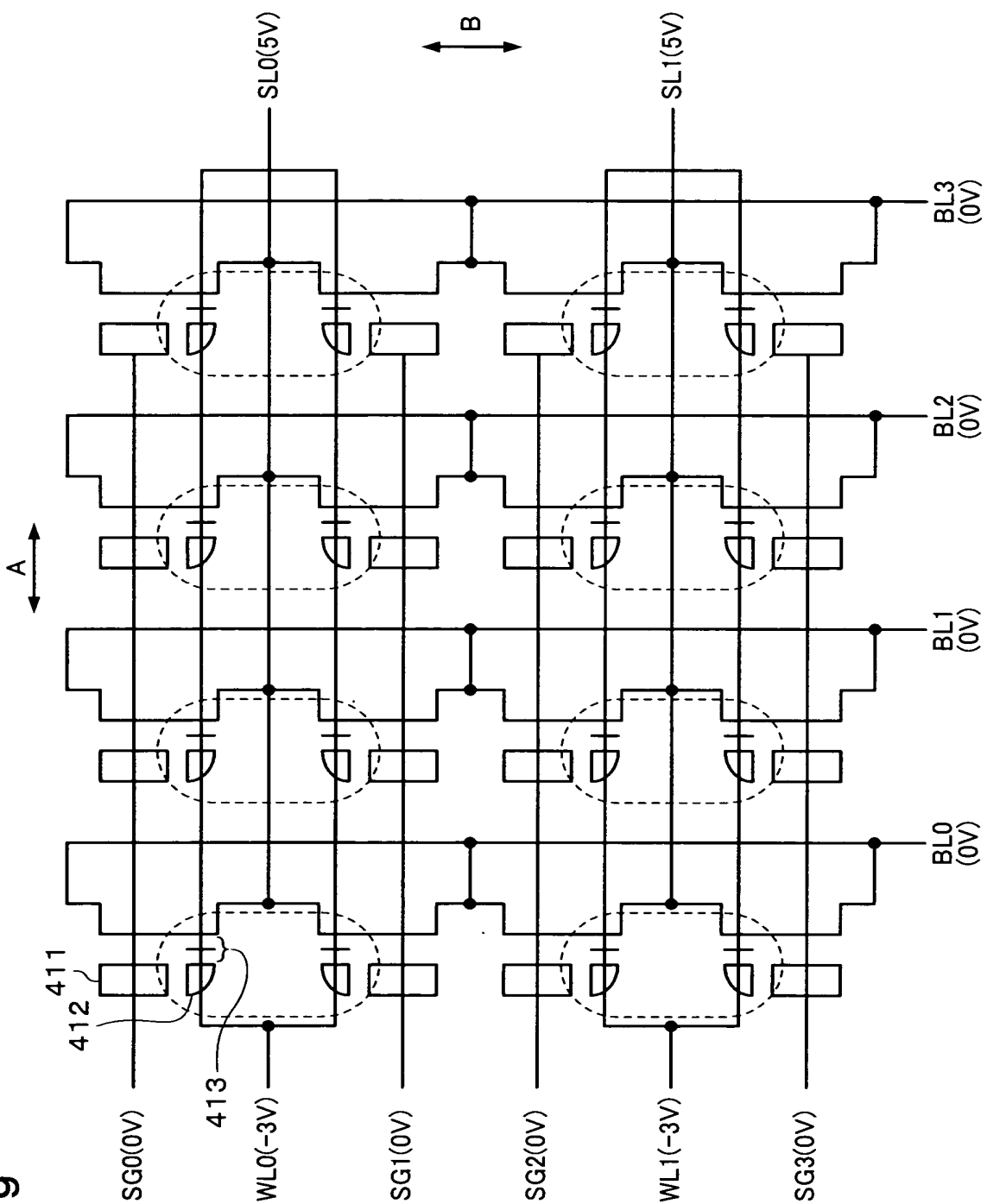




FIG. 10

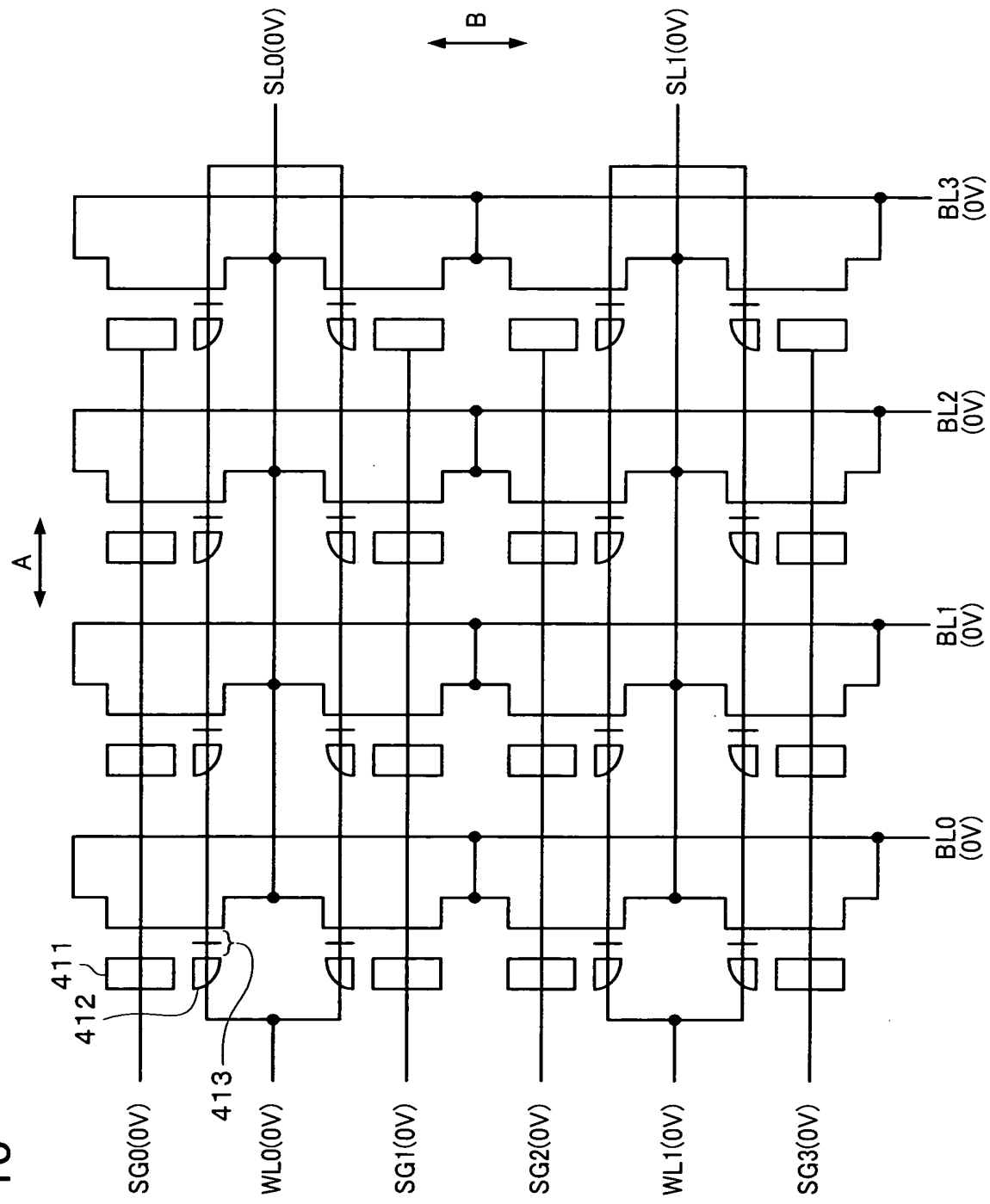


FIG. 11

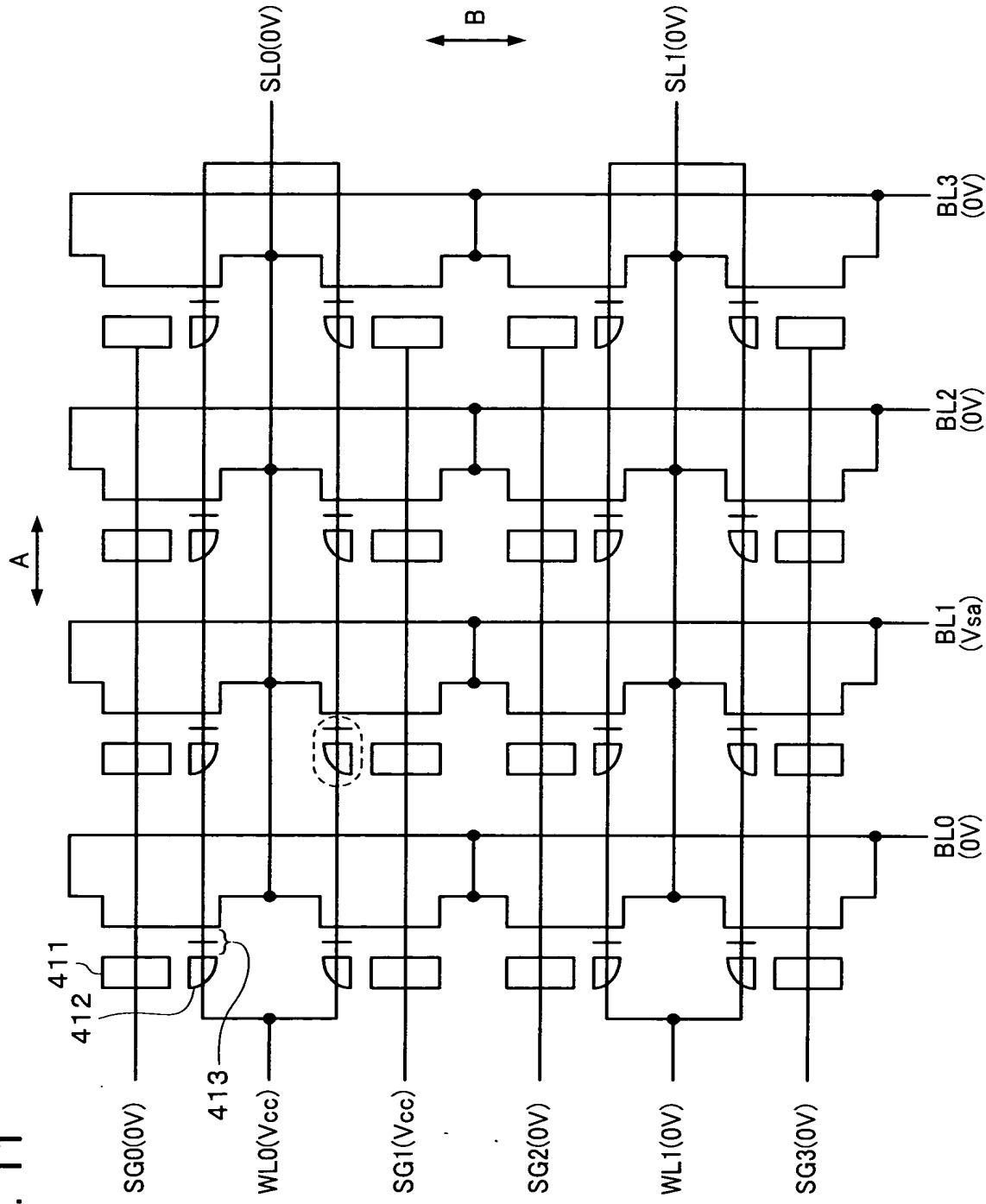


FIG. 12

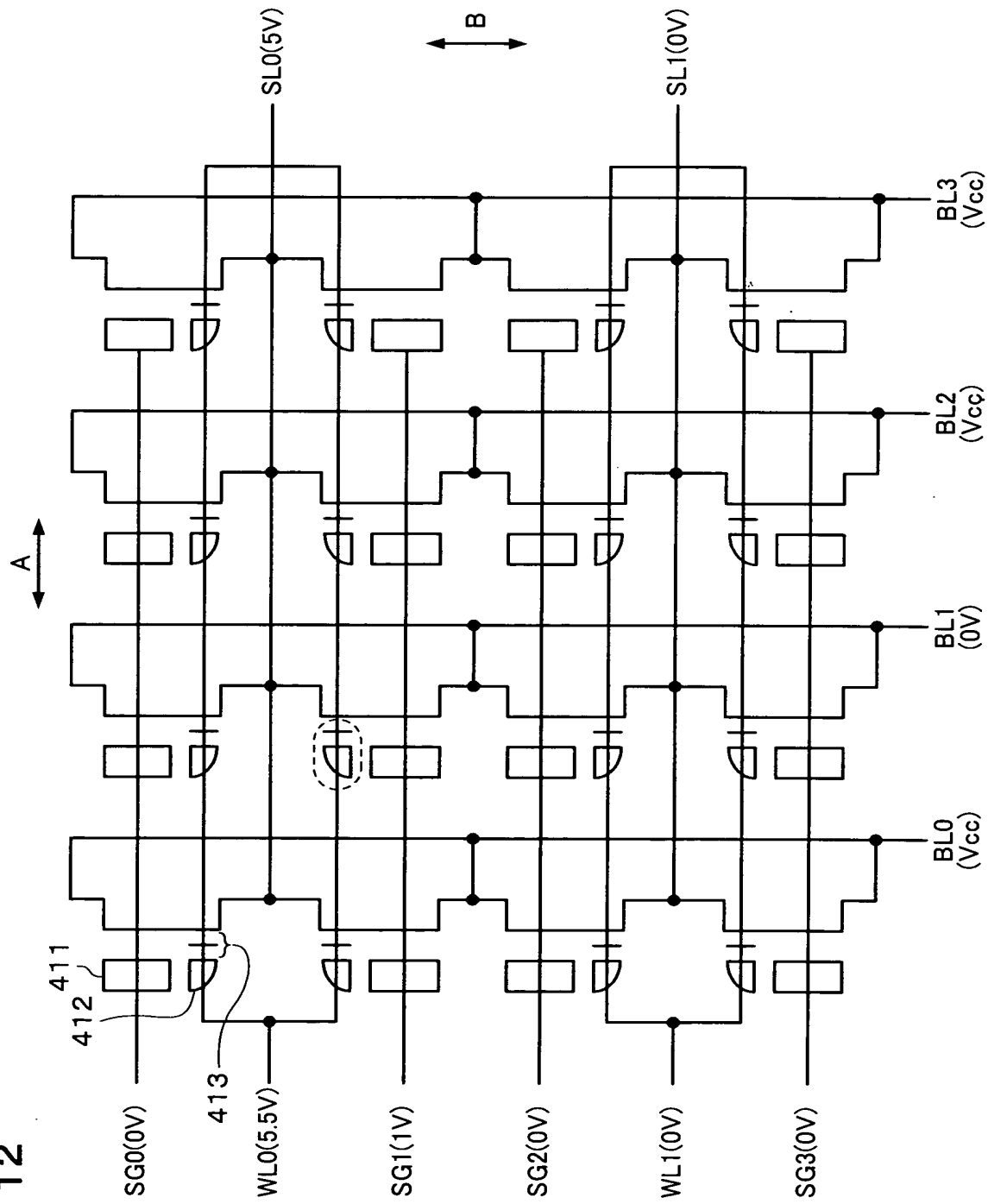


Figure 13 is a schematic diagram of a semiconductor device layout, showing a grid of word lines (WL0, WL1) and bit lines (BL0, BL1, BL2, BL3). The layout includes various electrical components like capacitors and transistors, with labels for signal levels (e.g., SL0(5V), WL0(-3V), SG0(0V)). Dimensions A and B are indicated.

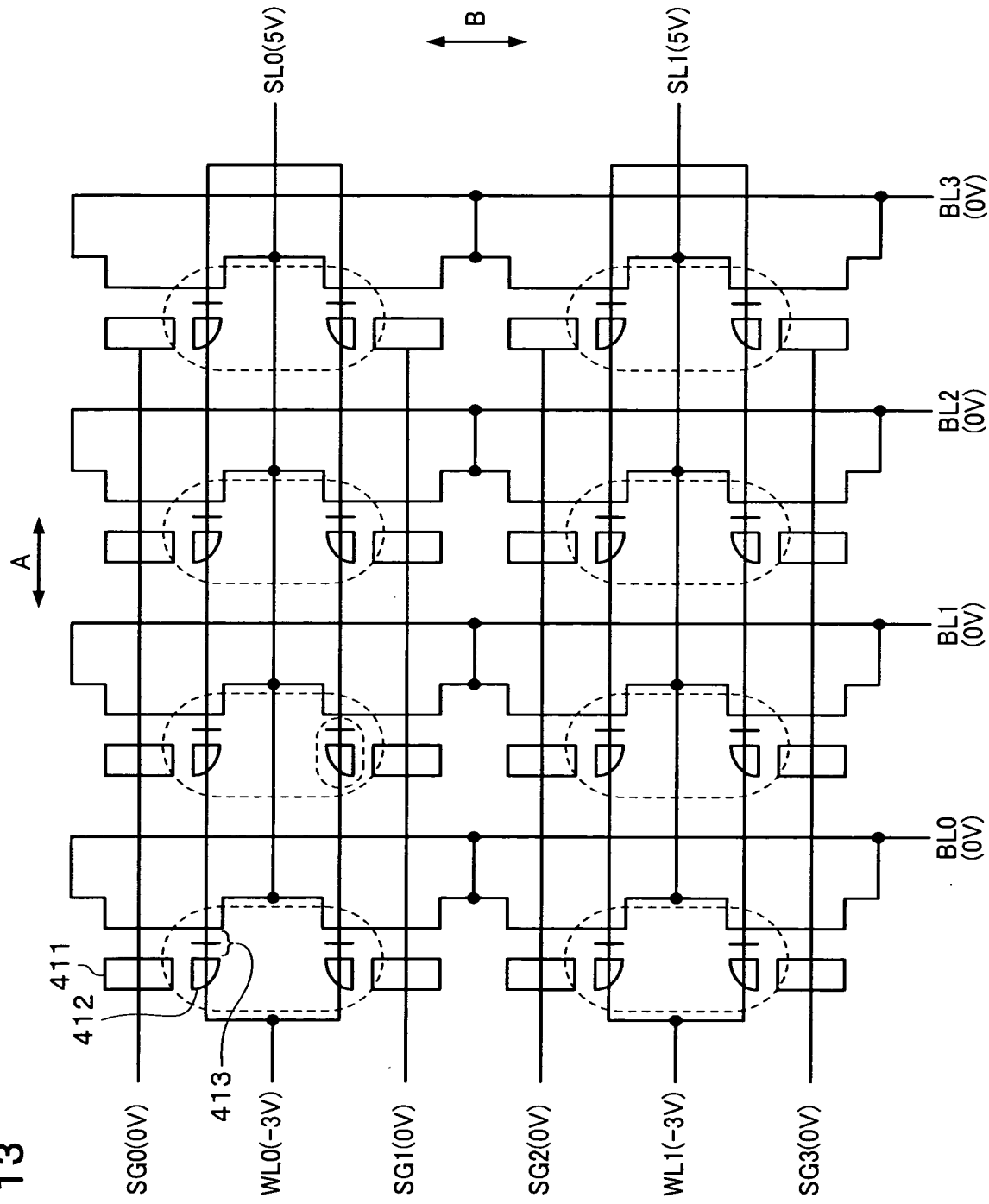


FIG. 14

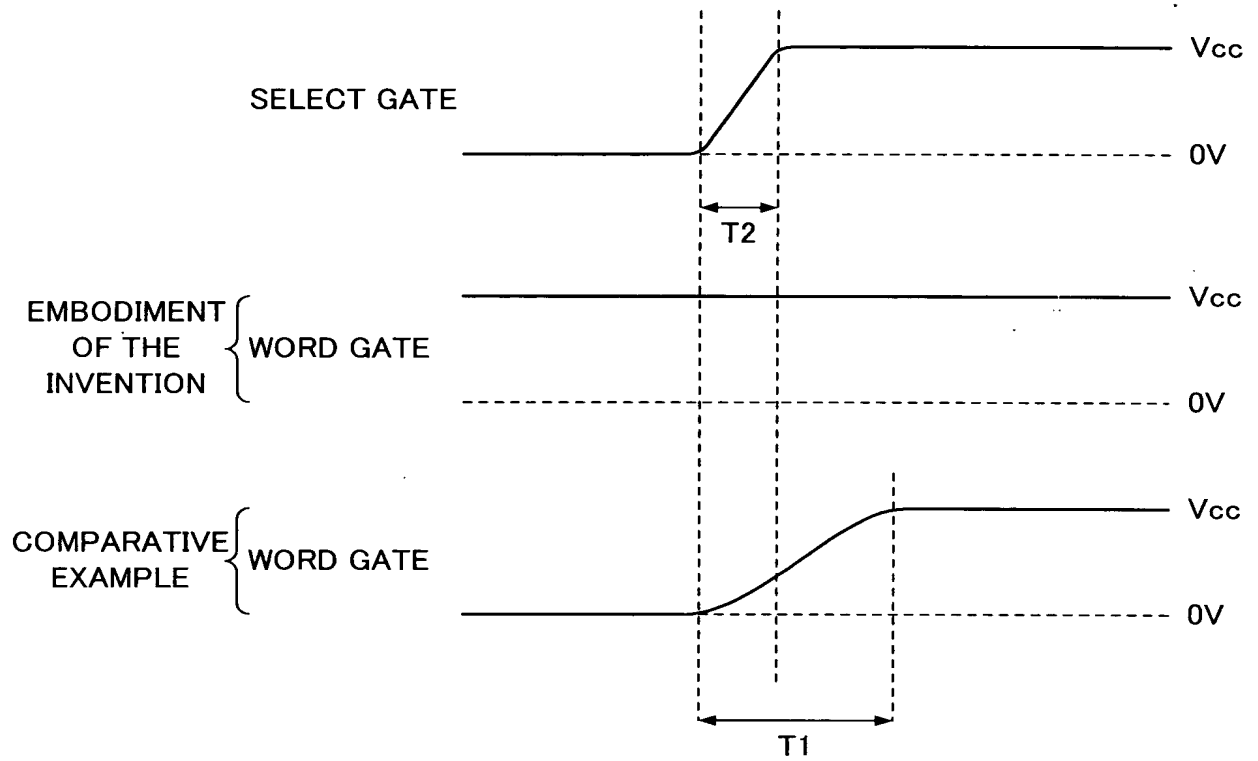


FIG. 15

